

REMARKS

Claims 1-4 and 6-12 are pending. Claims 13-25 have been withdrawn from consideration. New claims 26-28 are added. In accordance with the foregoing, claims 1, 8, and 12 are amended. Claim 11 is cancelled without prejudice or disclaimer of the subject matter contained therein. The specification has been amended to correct a typographical error. In the above referenced Office Action, claims 1-4 and 6-12 stand rejected. Applicant respectfully traverses the rejections and requests a withdrawal of all rejections as set forth below.

Claims 1-4 and 6-12 stand rejected under 35 U.S.C. 112, second paragraph as being indefinite. In accordance with the foregoing amendments, Applicant has corrected claim 1 to positively claim the high voltage termination region and respectfully requests withdrawal of the rejection.

Claims 1-4 and 6-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nishi (U.S. 5,949,140). Claim 1, as amended, recites "a backside contact coupling to the first electrode of the power transistor comprising at least one deep trench etched through the epitaxial layer, the deep trench extending from the epitaxial layer top surface to the semiconductor substrate and exposing the semiconductor substrate top surface wherein the at least one deep trench is etched in an area outside the high voltage termination region." Nishi purportedly teaches a deep trench by virtue of teaching a via hole 42. The via hole 42 is clearly shown to penetrate completely through the substrate 58, element separation region 64 and SiN layer 68 reaching the rear surface of the drain wiring 36a. The via hole 42 thus allows a metal to metal contact of via hole wiring to couple connecting wires on the top surface to rear electrodes on the rear surface. Applicant respectfully submits that via hole 42 is physically and functionally different than the claimed deep trench. Nonetheless, Applicant has amended claim 1 to clearly set forth the deep trench exposing a top surface of the semiconductor substrate. Clearly the via hole 42 of Nishi completely penetrates the substrate and does not expose a top surface of a semiconductor substrate. For at least this reason, the rejection should be withdrawn.

Applicant respectfully traverses the Examiner's assertion that it is well known in the implantable device arts to utilize a transistor, such as the one taught by Nishi in implantable defibrillators. Applicant submits that the transistor taught by Nishi is not a high voltage power transistor and would not function as needed in an implantable defibrillator.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello (U.S. 5,914,522) in view of Brendel (U.S. 2003/0213605). Aiello discloses a power semiconductor structure. Aiello fails to teach, among other things, a deep trench etched through the epitaxial layer exposing the semiconductor substrate. Brendel is relied upon for disclosing the trench. New affidavits will be timely filed showing the claimed structure was invented prior to the filing date of Brendel. Furthermore, as stated in previous responses, incorporated herein by reference, Brendel relates to a feedthrough filter terminal and is unrelated to a high voltage power transistor. The Brendel reference is irrelevant making it non-obvious to one having ordinary skill in the art to combine the teachings of Brendel relating to a feedthrough with the teachings of Aiello relating to a power transistor. Moreover, it is unclear what feature in the teachings of Brendel the Examiner is interpreting as a deep trench etched in an epitaxial layer exposing a semiconductor substrate. Brendel teaches a gold braze surrounding leads extending through an insulating material area. The insulating material area is formed in an aperture of a conductive ferrule 318. The ferrule is formed with a channel for facilitated assembly with a test fixture or housing of an implantable medical device. The channel along the periphery of the ferrule only exposes the conductive material of the ferrule. A deep trench etched through an epitaxial layer overlying a semiconductor substrate is not shown or taught. The applicant respectfully asserts the rejection is improper and should be withdrawn.

Applicant respectfully asserts that the present claims are in condition for allowance. Withdrawal of the instant rejections and issuance of a Notice of Allowance is respectfully requested.

Respectfully submitted,

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Date

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